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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/146,259	09/03/1998	TOYOHIKO YOSHIDA	028433-007	7001

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BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
TREAT, WILLIAM M	24
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/146,259	Yoshida et al.
Examiner	**Group Art Unit**
W. TREAT	2183

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on ~~Paper #~~ 5/6/02.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-25 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-25 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on [redacted] is ☐ approved ☐ disapproved.

☒ The drawing(s) filed on 9/3/98 is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

1. Claims 1-25 are presented for examination.

2. In view of the Supplemental Appeal Brief filed on 5/6/02, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Consider first that applicants have offered no consistent definition for the term, "instruction", anywhere in their specification and that they have used the term in multiple inconsistent ways throughout their disclosure. For example, "In the **instruction** formats, there are included a format 101 of dual **operation instruction** which designates two **operations** by one

instruction word as shown in Figure 2a and a format 102 of single **operation instruction** which designates one **operation** by one **instruction** word as shown in Figure 2b" (p. 21, line 27 through p. 22, line 6), or "In this program, a pair of **sub-instructions** in each row is described by a dual **operation instruction** 101 having the instruction format shown in Figure 2a, wherein **sub-instructions** I01, I11, I21, I31, I41, I51, and I61 are described in the **operation** field 106 as **operation**_0 and **sub-instructions** I02, I12, I22, I32, I42, I52, and I62 are described in the **operation** field 107 as **operation**_1" (p. 50, line 5-12), or "The **sub-instruction** I01 is a branch **instruction** BRA ..." (p. 50, line 18), or "The **sub-instruction** I21 is an add **instruction** ADD ..." (p. 50, lines 25-26), or "The **sub-instruction** I31 is a comparison **instruction** CMPEQ ..." (p. 51, lines 1-2). If one of ordinary skill in the art seeking to understand applicants' invention looks to applicants' specification, *supra*, for guidance as to how to determine what the invention requires in terms of an instruction he gets only conflicting advice. There are VLIW instructions (i.e. dual operation instruction 101 and single operation instruction 102) which can contain one or two operations which are equivalent to sub-instructions which are also instructions but instructions which cannot contain other instructions. So an instruction might contain one or two instructions or an instruction might not be able to contain any instructions.

6. Consider what happens when one of ordinary skill accepts applicants' argument that "their claims are written to encompass both the dual operation instruction and the single operation instruction," and that the examiners insistence their claims must distinguish between the properties of VLIW instructions and sub-instructions is irrelevant and then seeks to understand applicants'

invention of claim 1. If the first instruction to execute is a single operand instruction or sub-instruction represented by appellants' MULHX instruction (multiply with extended precision, p. 38, line 27 through p. 39, line 1), an instruction found in conventional superscalar or VLIW or multithreaded processors, the decoding and output by the decoder of a first control signal in a first period (claim 1, lines 8-9) is done in a rather predictable period though some computer companies have used a combination of fast and slow decoders and other gimmicks which make this period variable. However, the duration of the second period is indeterminate if one measures from the time when the instruction is decoded until when the execution of the instruction completes because modern superscalar, VLIW, and multithreaded processors typically decode instructions and then send the resultant information to what are frequently referred to as reservation stations to await the retrieval of operands and the freeing of the resources necessary to execute the instruction which can vary from immediately to several instruction cycles because of the mix of instructions executing, efficiency of the cache, exceptions, etc. Even just the time to execute a multiplication with extended precision can vary widely from processor to processor depending on the efficiency of the multiplication hardware. So the "second period" represents a highly variable period for which applicants disclosure provides little guidance and when one considers the difference in time between a multiplication with extended precision and a simple integer addition (the multiplication instruction invariably representing several multiples of the time for the addition), one of ordinary skill has no guidance to reconcile the widely variant interpretations of the "second period" when trying to understand applicants' claimed invention. The whole situation

becomes even more complicated if one accepts that the first instruction could be equivalent to a dual operation instruction, as applicants argue. The first period could be relatively determinant since the system has two decoders which may work simultaneously thereby limiting the variation in the first period to the issues discussed in relation to the single operation decode. However, there is no guidance as to how one calculates the second period for a dual operation instruction. Is it the sum of the execution periods for the two operations or the largest or the smallest, etc? It sure seems like applicants, by insisting there is no limitation to the term instruction and by refusing to narrow it in any way, are forcing ambiguity on their claims which render them unclear (i.e. they have a 112, 2nd problem), but applicants are entitled to assert what their interpretation of their claims is even if it renders them unpatentable. With the second period indeterminate based on the insufficiency of applicants' disclosure and their repeated insistence an instruction shall be interpreted as any form of instruction, the starting time for the fourth period, defined as "being started after elapsing a same time as said second period or longer from an ending of said third period" (claim 1, lines 18-20), becomes indeterminate (i.e. one of ordinary skill doesn't know what claim 1 is claiming).

7. Applicants' other claims have similar problems based on the ambiguity of terms such as instruction.

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to

> make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The fact that certain capabilities are provided to the invention by the format of the VLIW instruction while other capabilities are provided by the format of the sub-instructions of the VLIW instruction is critical or essential to the practice of the invention, but not included in the claim(s), is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

10. Applicants' claims mix the capabilities of instructions and sub-instructions without distinguishing as to what provides the capabilities and implying applicants have some form of hybridized instructions which are not enabled.

11. Consider first that applicants have offered no consistent definition for the term, "instruction", anywhere in their specification and that they have used the term in multiple inconsistent ways throughout their disclosure. For example, "In the **instruction** formats, there are included a format 101 of dual **operation instruction** which designates two **operations** by one **instruction** word as shown in Figure 2a and a format 102 of single **operation instruction** which designates one **operation** by one **instruction** word as shown in Figure 2b" (p. 21, line 27 through p. 22, line 6), or "In this program, a pair of **sub-instructions** in each row is described by a dual **operation instruction** 101 having the instruction format shown in Figure 2a, wherein **sub-instructions** I01, I11, I21, I31, I41, I51, and I61 are described in the **operation** field 106 as **operation**_0 and **sub-instructions** I02, I12, I22, I32, I42, I52, and I62 are described in the

operation field 107 as **operation_1**" (p. 50, line 5-12), or "The **sub-instruction** I01 is a branch **instruction** BRA ..." (p. 50, line 18), or "The **sub-instruction** I21 is an add **instruction** ADD ..." (p. 50, lines 25-26), or "The **sub-instruction** I31 is a comparison **instruction** CMPEQ ..." (p. 51, lines 1-2). If one of ordinary skill in the art seeking to recreate applicants' invention looks to applicants' specification, *supra*, for guidance as to how to determine what the invention requires in terms of an instruction he gets only conflicting advice. There are VLIW instructions (i.e. dual operation instruction 101 and single operation instruction 102) which can contain one or two operations which are equivalent to sub-instructions which are also instructions but instructions which cannot contain other instructions. So an instruction might contain one or two instructions or an instruction might not be able to contain any instructions. And, applicants can see no problems for one of ordinary skill seeking to recreate their invention.

12. Consider what happens when one of ordinary skill accepts applicants' argument that "their claims are written to encompass both the dual operation instruction and the single operation instruction," and that the examiners insistence their claims must distinguish between the properties of VLIW instructions and sub-instructions is irrelevant and seeks to recreate applicants' invention of claim 1. First, it would seem one could not build a modern superscalar or VLIW or multithreaded processor which conformed to the limitations of claim 1. If the first instruction to execute is a single operand instruction or sub-instruction represented by applicants' MULHX instruction (multiply with extended precision, p. 38, line 27 through p. 39, line 1), an instruction found in conventional superscalar or VLIW or multithreaded processors, the decoding and output

by the decoder of a first control signal in a first period (claim 1, lines 8-9) is done in a rather predictable period though some computer companies have used a combination of fast and slow decoders and other gimmicks which make this period variable. However, the duration of the second period is beyond the system designers control if one measures from the time when the instruction is decoded until when the execution of the instruction completes because modern superscalar, VLIW, and multithreaded processors typically decode instructions and then send the resultant information to what are frequently referred to as reservation stations to await the retrieval of operands and the freeing of the resources necessary to execute the instruction which can vary from immediately to several instruction cycles because of the mix of instructions executing, efficiency of the cache, exceptions, etc. Even just the time to execute a multiplication with extended precision can vary widely from processor to processor depending on the efficiency of the multiplication hardware. So the "second period" represents a highly variable period for which applicants disclosure provides little guidance and when one considers the difference in time between a multiplication with extended precision and a simple integer addition (the multiplication instruction invariably representing several multiples of the time for the addition), the system designer has no guidance to reconcile the widely variant interpretations of the "second period" when trying to recreate applicants' claimed invention. The whole situation becomes even more complicated for the system designer trying to replicate applicants' invention if one accepts that the first instruction could be equivalent to a dual operation instruction, as applicants argue. The first period could be relatively determinant since the system has two decoders which may work

simultaneously thereby limiting the variation in the first period to the issues discussed in relation to the single operation decode. However, the system designer now has no guidance as to how one calculates the second period for a dual operation instruction. Is it the sum of the execution periods for the two operations or the largest or the smallest, etc? It sure seems like applicants, by insisting there is no limitation to the term instruction and by refusing to narrow it in any way, are forcing ambiguity on the system designer which renders him unable to recreate their invention (i.e. they have a 112, 1st problem), but applicants are entitled to assert what their interpretation of their claims is even if it renders them unpatentable. With the second period indeterminate based on the insufficiency of applicants' disclosure and their repeated insistence an instruction shall be interpreted as any form of instruction, the starting time for the fourth period, defined for the systems designer as "being started after elapsing a same time as said second period or longer from an ending of said third period" (claim 1, lines 18-20), becomes indeterminate (i.e. one of ordinary skill doesn't know how to recreate applicants' invention).

13. Applicants' other claims have similar problems based on the ambiguity of terms such as instruction.

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-25 are rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Holmann et al. (Japanese Application No. JP08203675).

17. As noted in the examiner's previous actions, applicants' severe 112 problems make it unclear how to best apply Holmann. However, despite these problems, the examiner will attempt to point out relevant anticipation and obviousness aspects of Holmann.

18. Using pseudocode the examiner will provide a small loop-execution program making use of the capabilities of Holmann's delayed branching instructions as set forth in his specification. Since a U.S. application is being examined, the examiner will use the U.S. Patent No. 5,815,698 as a translation of the specification and drawings of JP08203675 though it should be made clear this rejection relies upon the Japanese document being provided to applicants and on its earlier publication date of 2/20/98.

19. PSEUDO CODE PROGRAM

I1 Move Value to Counter (cols. 11 and 12)

I2 Move Ix to REG1 (cols. 11 and 12)

I3 BSET RP (i.e. make RP valid) (cols. 11 and 12 and col. 18, lines 45-60)

I4 DBRA When PC=REG1 to I4 (cols. 11 and 12 and col. 14, lines 10-20)

I5 Perform Computations

I6 Perform Computations, etc.

Ix-3 Subtract 1 from Counter (cols. 11 and 12)

Ix-2 BRATNZ to Ix testing Counter (cols. 11 and 12)

Ix-1 BCLR RP (i.e. make RP invalid) (cols. 11 and 12 and col. 18, lines 45-60)

Ix Further Processing...

The program performs a loop the number of times set initially in Counter using the DBRA instruction which branches back to itself when the PC equals the address of instruction Ix. It does this as long as the condition RP=1 holds. When the condition changes to RP=0, it does not loop back.

20. In light of paragraph 19, *supra*, let us consider how Holmann anticipates applicants' claim 14. Holmann certainly has all the hardware of the processing device being claimed (Figs. 5 and 12). He saves the value of the program counter to be used to compare against the PC in a first register (col. 14, lines 25-45) as applicants claim, and the hardware faithfully checks to see if the condition (RP is valid or invalid) as a condition of executing the branch.

21. As to claim 15, it merely says the value selected to be compared against the PC can be variable which Holmann teaches (col. 20, lines 8-15).

22. As to claim 16, it fails to teach or define over rejected claims 14-15 in any significant way.

23. As to claim 18-20, if the conditions of claims 18-20 hold true, then the instruction of claim 14 must inherently be a dual operation instruction and applicants' assertion that it could be a single operation instruction is inconsistent with applicants' specification.

24. As to claims 21 and 22, they fail to teach or define over rejected claims 14-16.

25. As to claim 23 and 24, if the conditions of claims 23 and 24 hold true, then the instruction of claim 21 must inherently be a dual operation instruction, and applicants' assertion that it could be a single operation instruction is inconsistent with applicants' specification.

26. As to how applicants' (for instance) delayed branch-not-equal-to-zero instruction would be obvious to one of ordinary skill in the art, I would again refer to the program of paragraph 19, *supra*. Unless one is an idiot in the art, one recognizes that the code at I4, Ix-2 and Ix-1 is a clumsy way to control the loop. If one makes the BRATNZ instruction capable of delayed operation, one eliminates two instructions thereby reducing the amount of code and speeding execution of the loop. Holmann taught delayed unconditional branching (col. 12). It would be obvious to one of ordinary skill extending that teaching to include delayed conditional branching would afford greater programming flexibility and would allow reduction in the number of instructions necessary for control of loops using delayed branching thereby speeding execution and reducing code storage requirements. Holmann already taught a dual operand instruction (Fig. 6a). Extending that to allow two delayed operations in the dual operation instruction is merely a logical extension of his concepts. Once one does that then the necessary registers to hold the appropriate data are necessary for the concept to work and represent no inventive concept.

27. As to applicants' claims 1-13 and 17, they, too, would then be rendered either obvious or anticipated were they not so ambiguous.

28. The subject matter of this application admits of illustration by a drawing to facilitate understanding of the invention. Applicant is required to furnish a drawing under 37 CFR 1.81. No new matter may be introduced in the required drawing.

29. In claims 14, 18, and 20 applicants make many determinations based on the data in registers and other elements and describe a specific sequence of events and timing relationships based on the data and determinations. The same holds true for other of their claims. Applicants have pointed out how parts of several drawings in conjunction with much of their specification will allow one to understand their drawings. The concept behind 37 CFR 1.81 is that the drawing itself, in the absence of the specification, will enable understanding of the claim and not that the drawings in conjunction with a 100 page specification will allow understanding of the claim.

30. The drawings are objected to because they lack suitable legends. 37 1.84(o) states: "Suitable descriptive legends may be used subject to approval by the Office, or **may be required** by the examiner where necessary for understanding of the drawing. They should contain as few words as possible." Applicants drawings contain roughly 46 registers only designated by numbers. Numbers convey no meaning in terms of the drawings elements relevance to any claim language. Without a search through applicants' specification the registers are just numbered blank boxes in a drawing with no known purpose. A proposed drawing correction or corrected

drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

31. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the material set forth in the examiner's previous actions as well as that designated in paragraph 29, *supra*, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

32. 37 CFR 1.83 reads as follows:

§ 1.83 Content of drawing.

(a) The drawing in a nonprovisional application **must show every feature** of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).

(b) When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

(c) **Where the drawings in a nonprovisional application do not comply with the requirements of paragraphs (a) and (b) of this section, the examiner shall require**

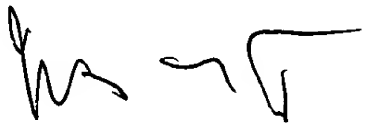
such additional illustration within a time period of not less than two months from the date of the sending of a notice thereof. Such corrections are subject to the requirements of § 1.81(d).

[31 FR 12923, Oct. 4, 1966; 43 FR 4015, Jan. 31, 1978; paras. (a) and (c) revised, 60 FR 20195, Apr. 25, 1995, effective June 8, 1995]

33. Applicants should note that the only provision for not providing a drawing depicting each claim element is when the elements are conventional (i.e. prior art). If applicants are prepared to argue that all claim elements not shown in their drawings, such as the determinations based on the various conditions being claimed, are prior art, the examiner would certainly drop the objection under 37 CFR 1.83(a).

34. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objections to the drawings will not be held in abeyance.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Treat whose telephone number is (703) 305-9699. The examiner works a flexible schedule, but he can normally be reached during the afternoons and evenings on four of the five weekdays.



WILLIAM M. TREAT
PRIMARY EXAMINER